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Summary of MoNA trigger time values for vtx_b8.bit:

TA = vme1=18 (3/30/05)=225ns
TB = vme2=6(3/30/05)=75ns
TC=vme1+vme2=300ns
TD=vme1+vme2+6=375ns
TE=vme1+vme2+6+vme3
TF=watchdog
TG=vme2+6=150ns

T0 = (TA after first MoNA) or (sweeper trigger) whichever comes first=assert veto
T1=T0 (not removed for backward compatibility)=calculate to level 1
T2=(TC after first MoNA) or (TB after sweeper trigger) whichever comes first=assert go if valid
T3=(TD after first MoNA) or (TG after sweeper trigger) whichever comes first=assert FC if not valid.
T4=(TE after first MoNA) or (TE after sweeper trigger) whichever comes first=end of FC wait time (while adcs settle). Really should be vme2+6+vme3 after sweeper trigger but this would require an even larger FPGA programming change. The settling time for events with no MoNA will be longer that needed.
T5=(TF after first MoNA or sweeper) whichever is first=watchdog timer. This is so long that there is no point in having different times for the two trigger paths.
T6=(TC after first MoNA) or (TB after sweeper)=TDC veto turn on time. Same as T2 but kept separate for historical reasons.

Setting the External and Internal delays:

VME1 and the external delay of the trigger work together. If the external delay of the trigger is too short, one will not realize the full coincidence window. If this external delay is too long then the timings of the system will be determined solely by the MoNA signals and if really too long, the coincidence condition will not be satisfied and events will be lost. If the vme1 is too long, then the time before fast clear will be longer than necessary and one could get events that were accepted by the logic but which were not timed to be accepted by the TDC. Note that the external delay will need to be adjusted as the velocity of the fragment through the magnet changes in different experiments.

VME2 is the time to wait in level 2 before checking to see if the event is valid and then giving a computer go. There is jitter of about 40ns. It seemed from the scope that a value of 3 was okay for this and so a minimum value of 4 has been adopted. As this is increased the time for the trigger back to the sweeper is increased. It should not be more than about 9 to meet the timing requirements of the sweeper.

VME3 is set by the properties of the VME modules so that the adcs can settle properly. Set to a value of 60 to get 750ns. Documentation says need 700ns.

The recommended way to set the two external delays is as follows:

1) check the values in the fpga gui (16, 18, 6, and 60).
2) make the external delay in the trigger path short (10ns or barrel the wires together for zero delay).
3) this should result in RAW TDC spectra that are cut in at the left (low channel side).
4) adjust the delay time for the common stop path so that the target gammas come at about channel 3750 (not less than 3600 and not more than 3840).
5) add delay to the trigger path until the RAW TDC spectra extend to channel 256-300. Do not add delay to the path beyond the point where this is observed. You can estimate this delay ahead of time. If our simulations are correct and the transit times in the phototubes match the datasheets then the needed delay is 81ns-fragment flight time from potscint to thin scint. If the flight time is longer than 81ns you will need a negative length cable or you will need to string a shorter, more direct cable between the sweeper and MoNA. (Shorter than 132ns.)

Note that be agreement with Daniel Bazin, the returned trigger should never arrive back at the sweeper more than 600ns after it leaves the sweeper. Currently, this time is 530ns. The sweeper electronics depends on having this returned valid event trigger (computer go) by this time for proper operation of the tracking CRDCs and sweeper CRDCs. This is approximately the time between the arrival of the sweeper trigger at the MoNA delay and the computer go out of the nim-ecl converter plus 280ns.
DON"T VIOLATE THIS RULE.